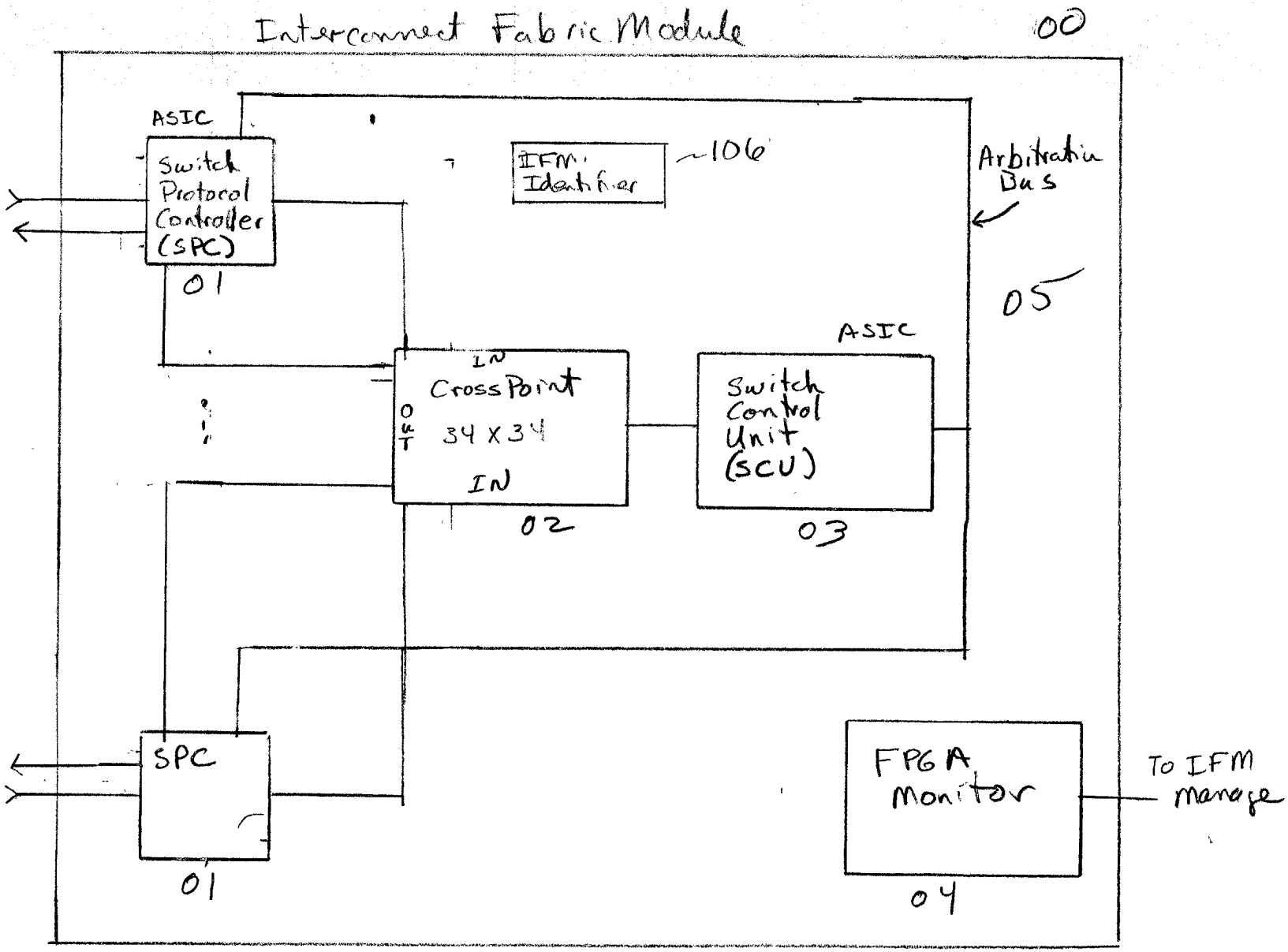

Interconnect Fabric Module
00
ASIC
Switch Protocol Controller (SPC)
01
IFM Identifier
106
Arbitration Bus
05
ASIC
IN
Cross Point
OUT
34 X 34
IN
02
Switch Control Unit (SCU)
03
SPC
01
FPGA Monitor
04
To IFM manage

Fig 1

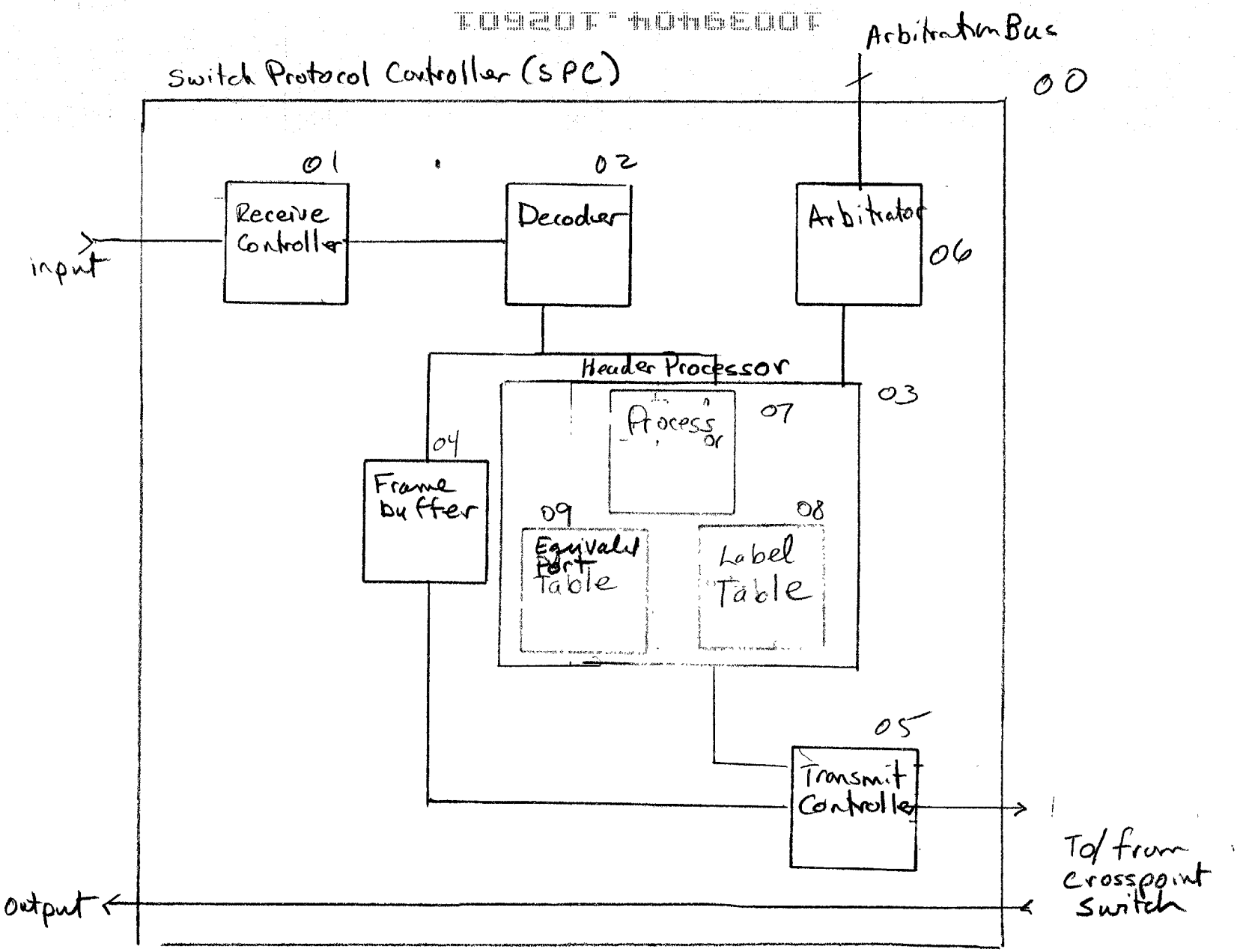

Switch Protocol Controller (SPC)
Arbitration Bus
00
01
02
Receive Controller
Decoder
Arbitrator
06
input
Header Processor
03
Process or
07
04
Frame buffer
09
08
Equivalent Port Table
Label Table
05
Transmit Controller
To/from crosspoint switch
output

Fig 2

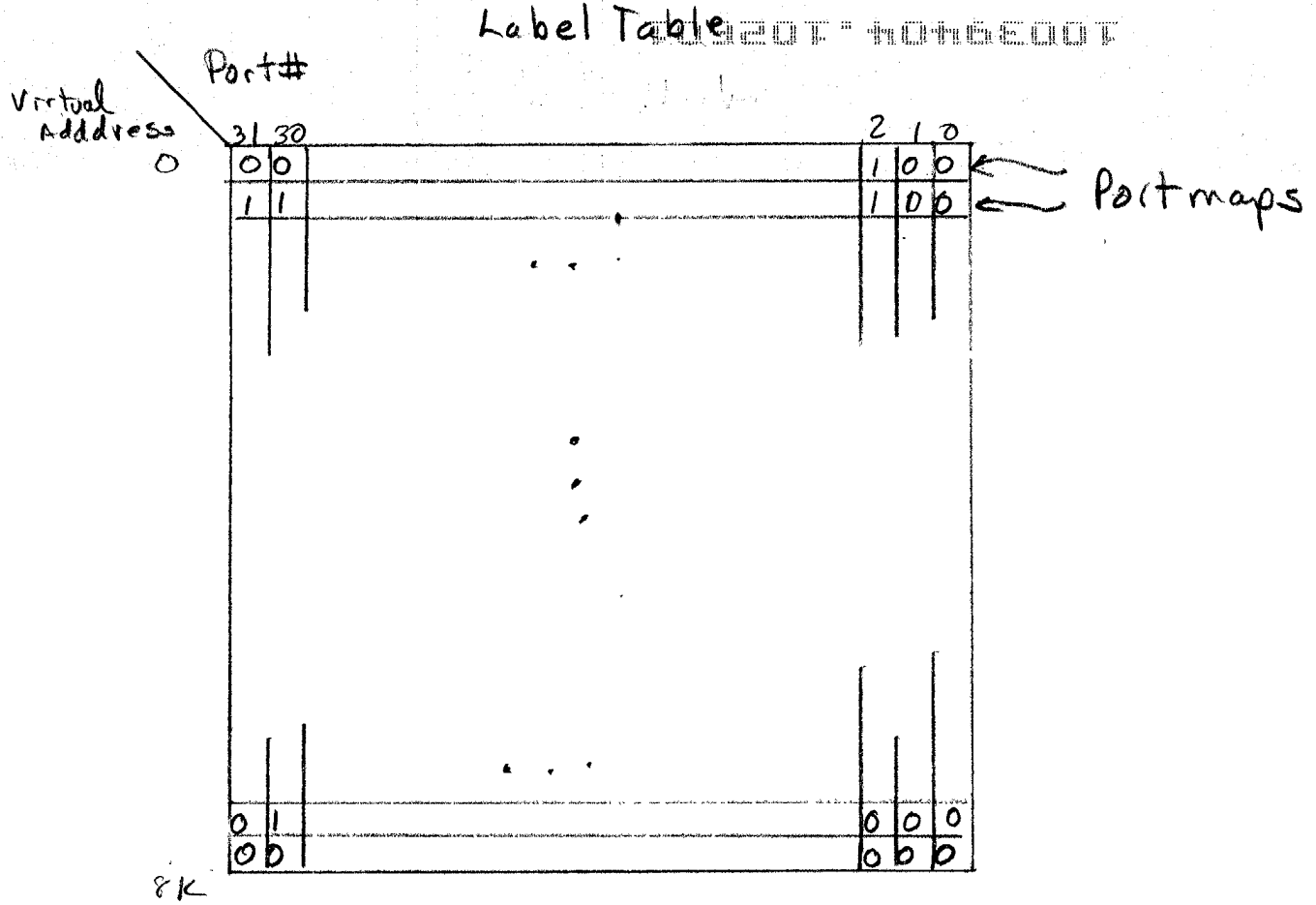

Label Table
Port#
Virtual Address
31 30
2 1 0
0
1 0 0
1 0 0
Portmaps
0 1
0 0
0 0 0
0 0 0
8K

Fig 3

Frame

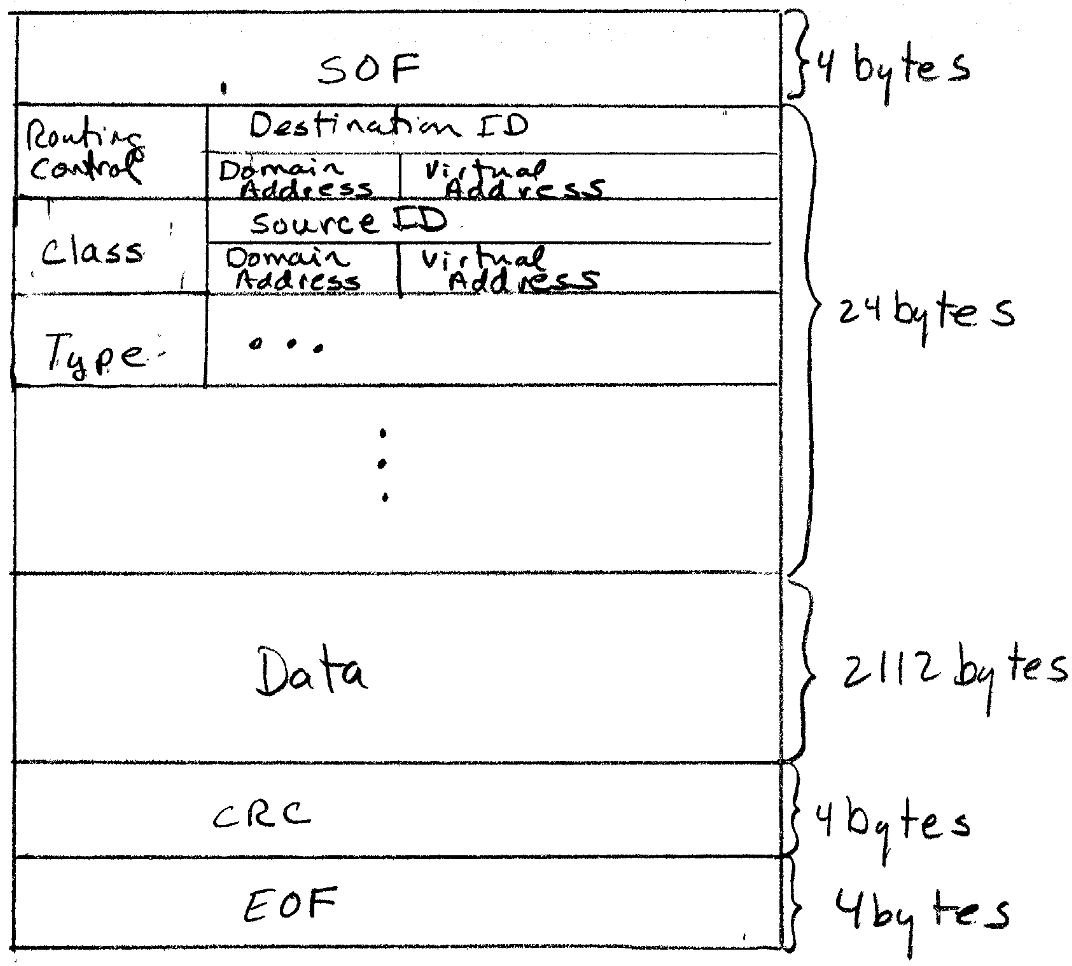

SOF
4 bytes
Routing Control
Destination ID
Domain Address
Virtual Address
Class
Source ID
Domain Address
Virtual Address
Type
24 bytes
Data
2112 bytes
CRC
4 bytes
EOF
4 bytes

Fig 4

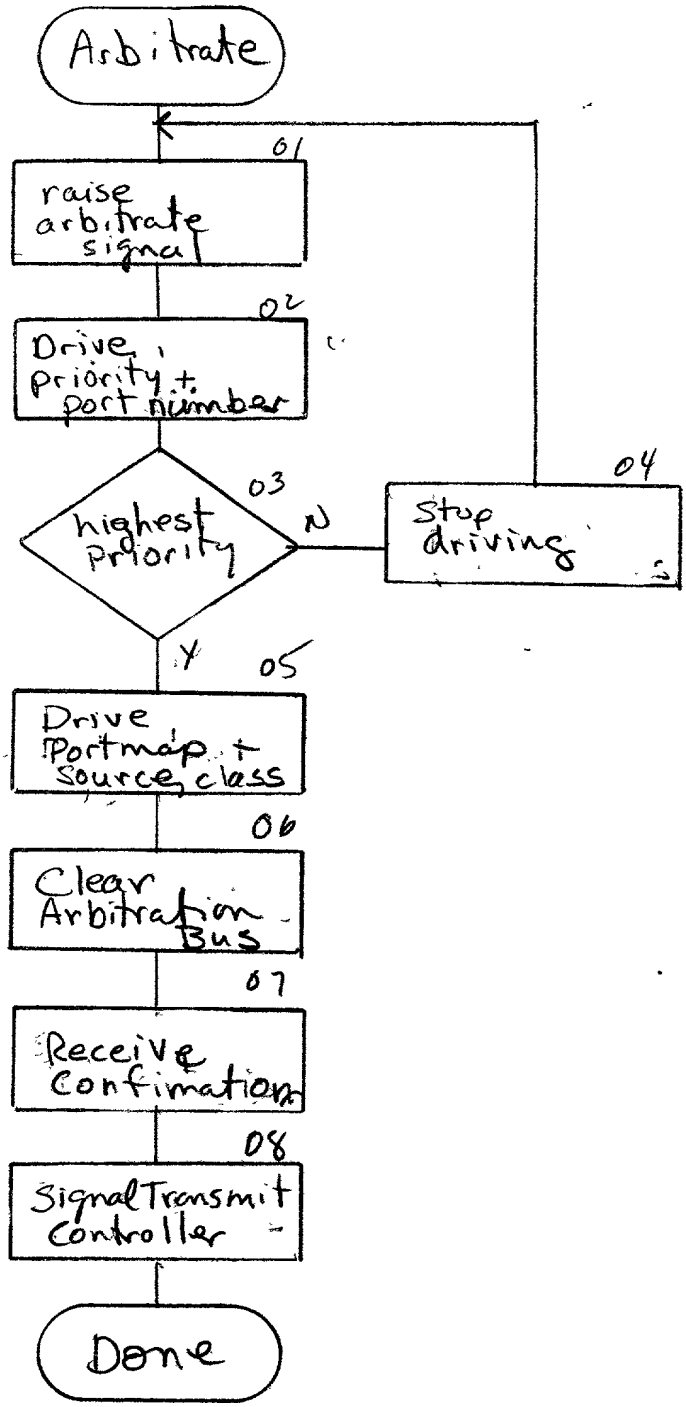

Arbitrate
01
raise arbitrate signal
02
Drive priority + port number
03
highest priority
N
04
Stop driving
Y
05
Drive Portmap + Source class
06
Clear Arbitration Bus
07
Receive Confimation
08
Signal Transmit Controller
Done

Fig 5

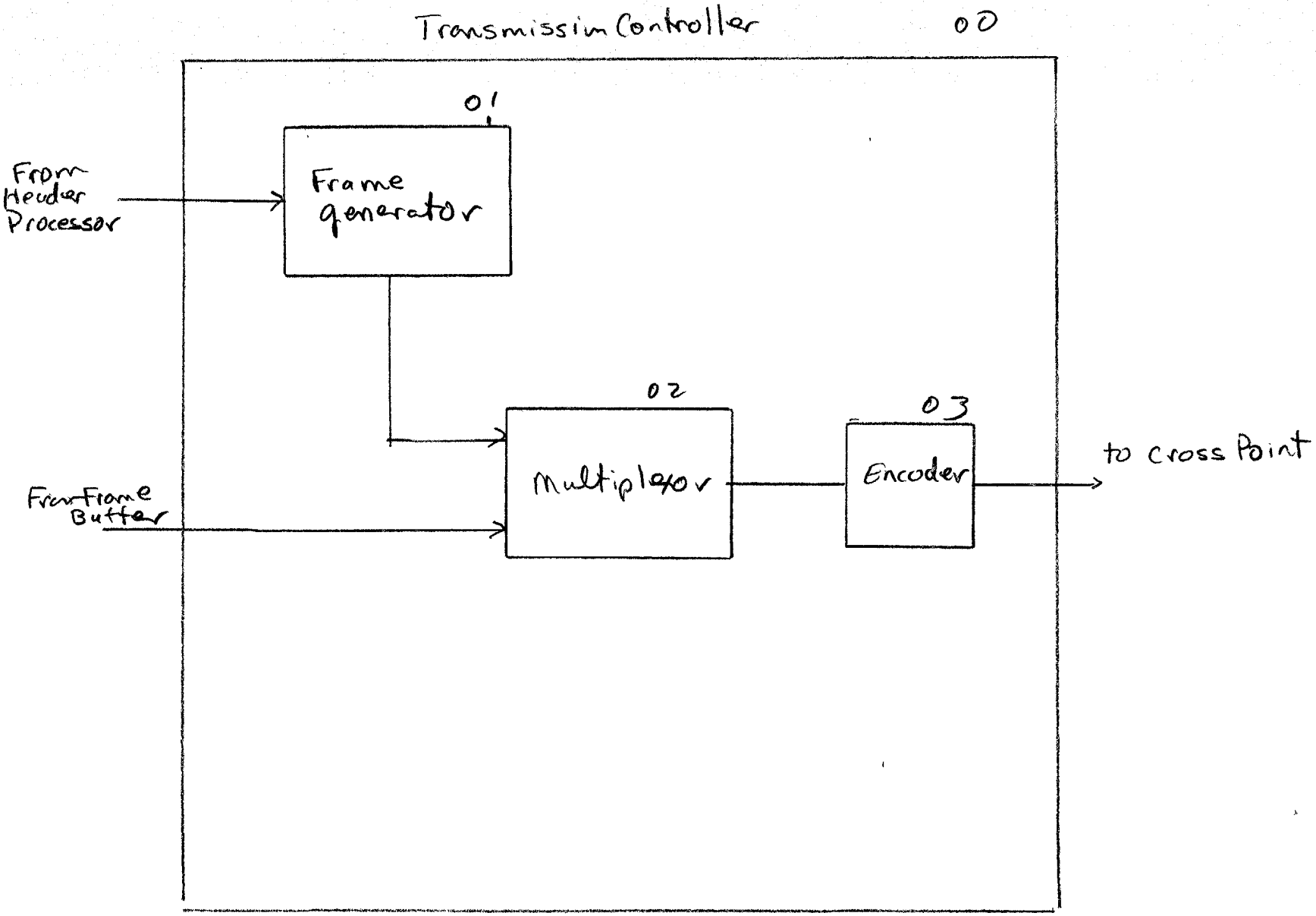


Fig 6

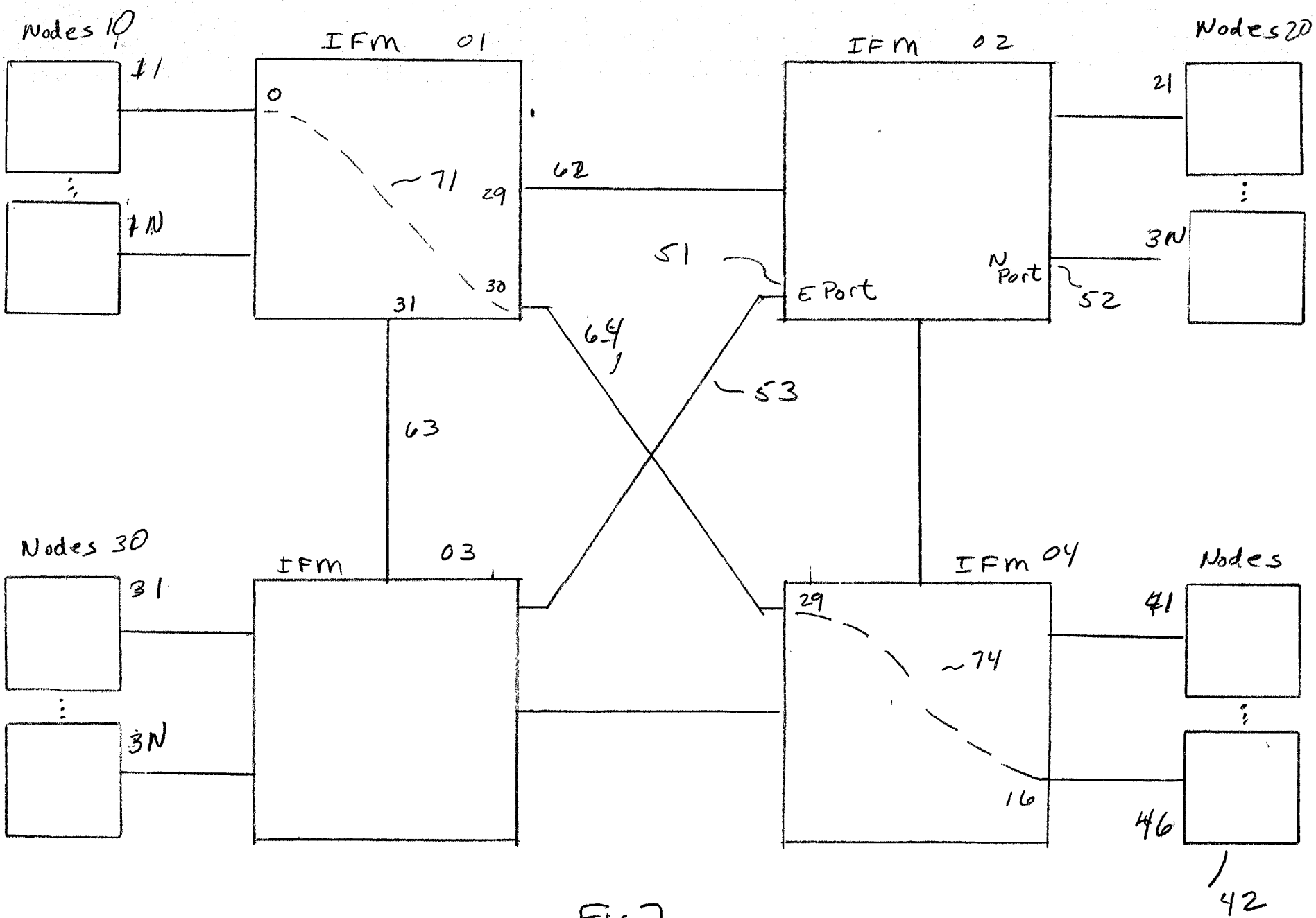


Fig 7

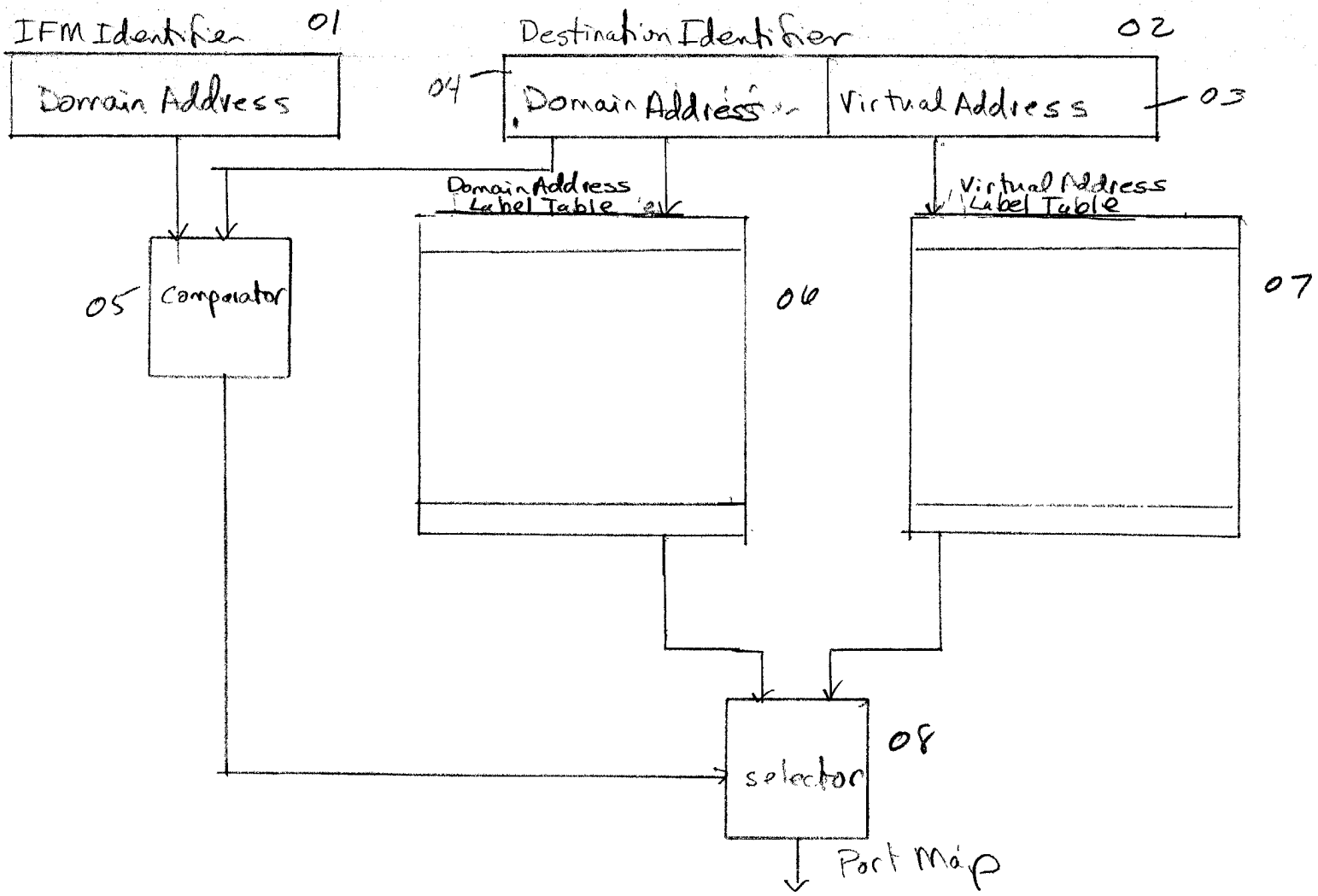

IFM Identifier
01
Domain Address
Destination Identifier
02
04
Domain Address
Virtual Address
03
Domain Address Label Table
Virtual Address Label Table
05
Comparator
06
07
08
selector
Port Map

Fig. 8

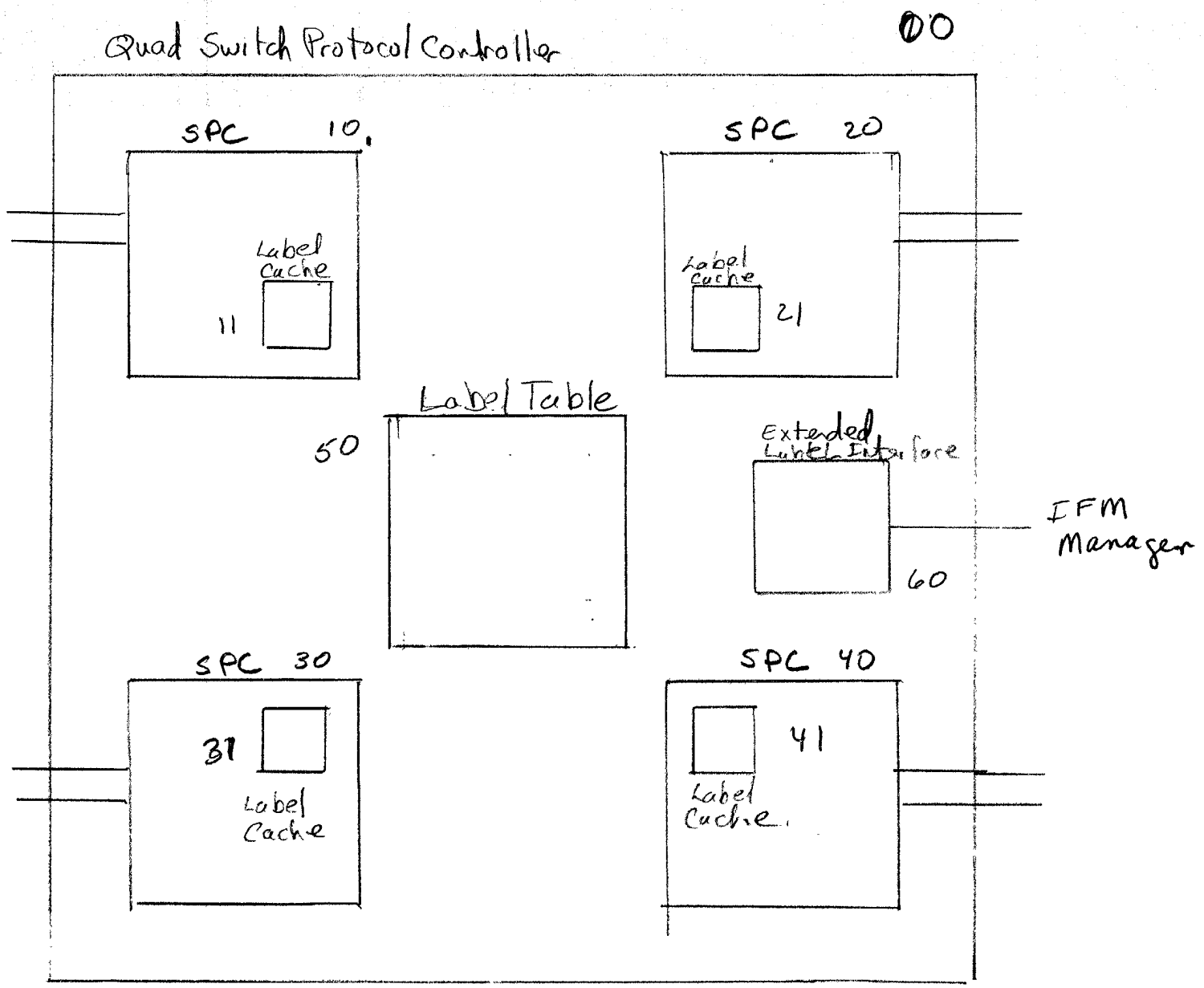

Quad Switch Protocol Controller
00
SPC 10
Label Cache
11
SPC 20
Label Cache
21
Label Table
50
Extended Label Interface
60
IFM Manager
SPC 30
31
Label Cache
SPC 40
41
Label Cache

Fig 9

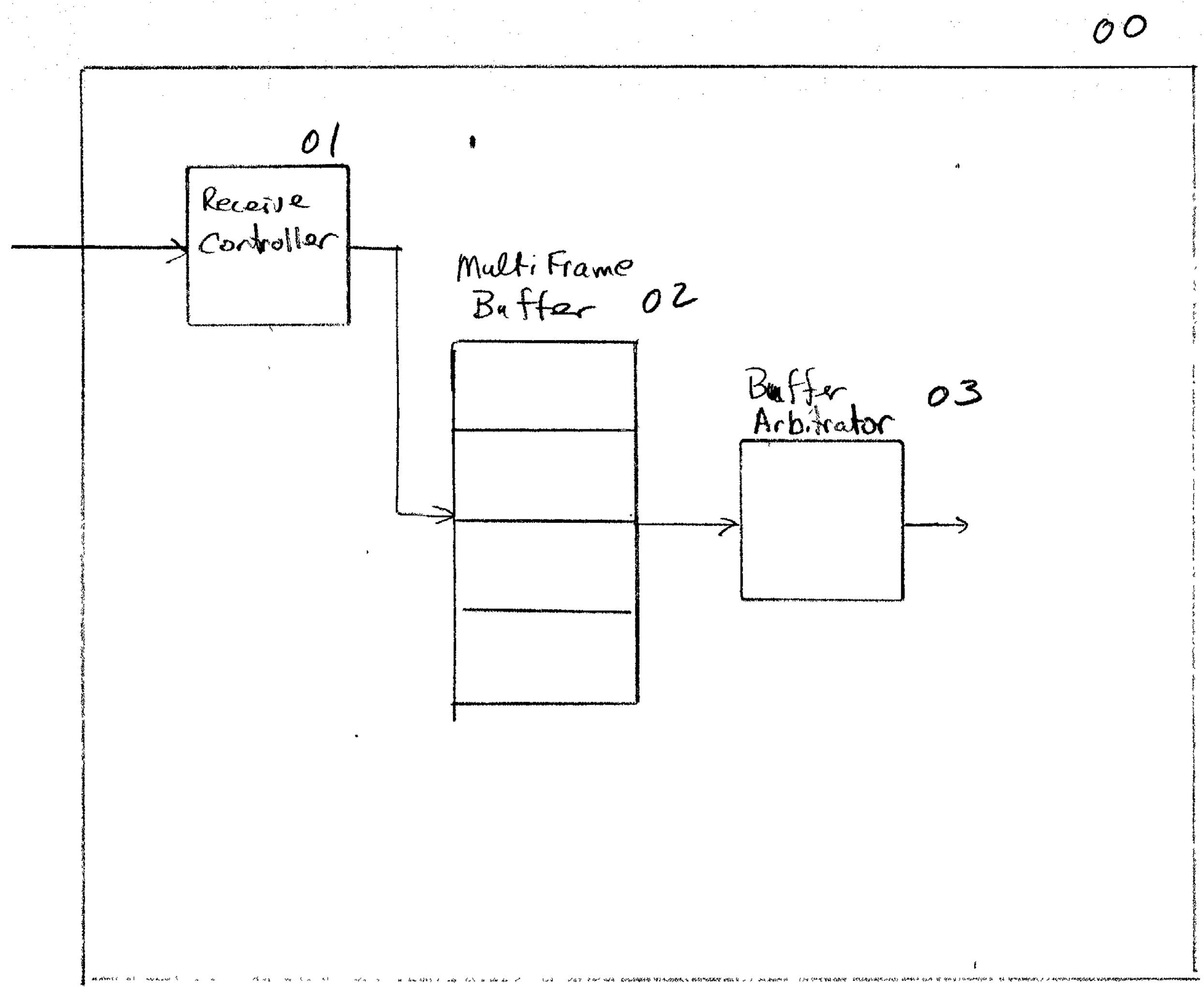

00
01
Receive Controller
Multi Frame Buffer
02
Buffer Arbitrator
03

Fig 10

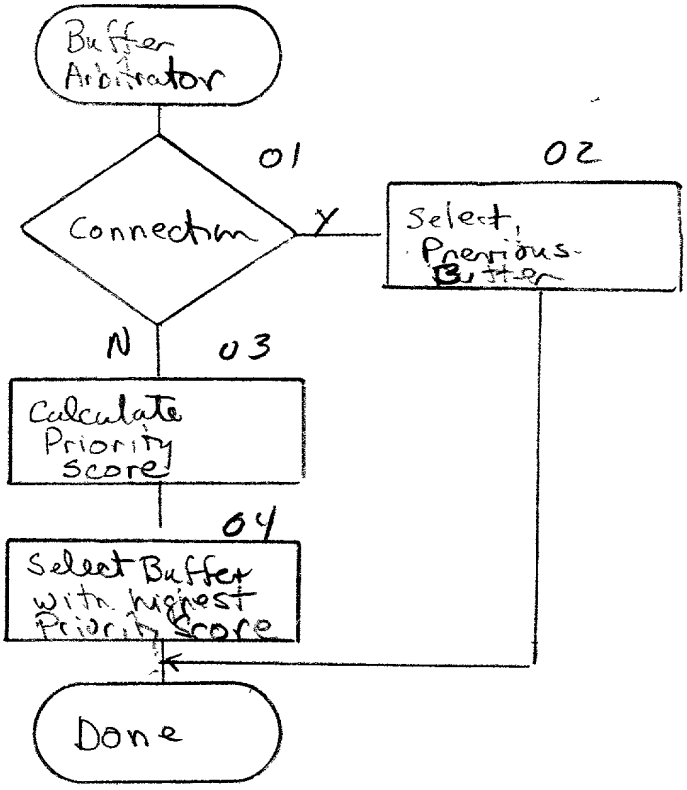

Buffer Arbitrator
01
02
Connection
Y
Select Previous Buffer
N
03
Calculate Priority Score
04
Select Buffer with highest Priority Score
Done

Fig 11

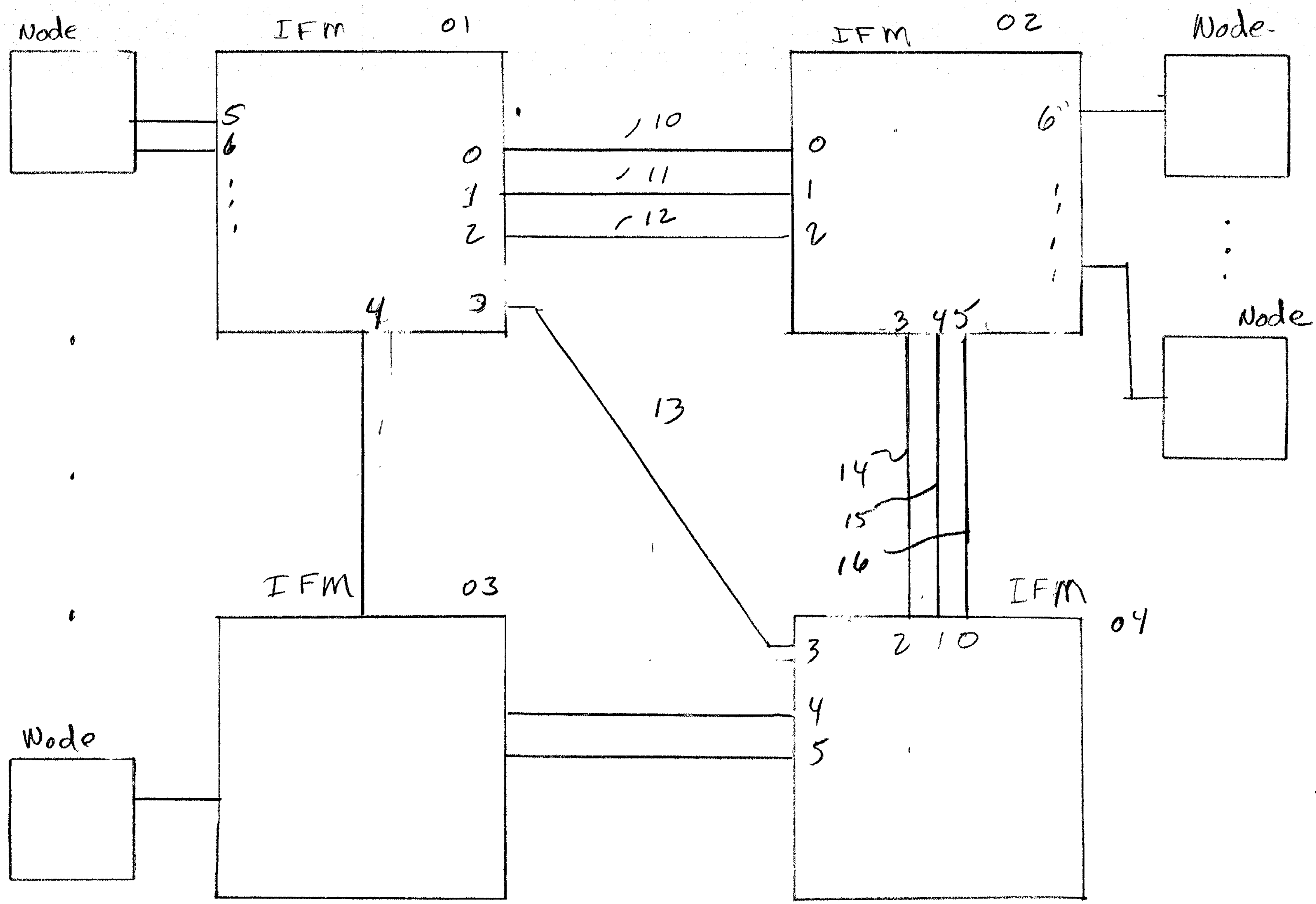

Node
IFM
01
5
6
0
1
2
3
4
/10
/11
/12
13
IFM
02
Node
6
0
1
2
3
4
5
Node
14
15
16
IFM
03
IFM
04
3
2
1
0
4
5
Node

Fig 12

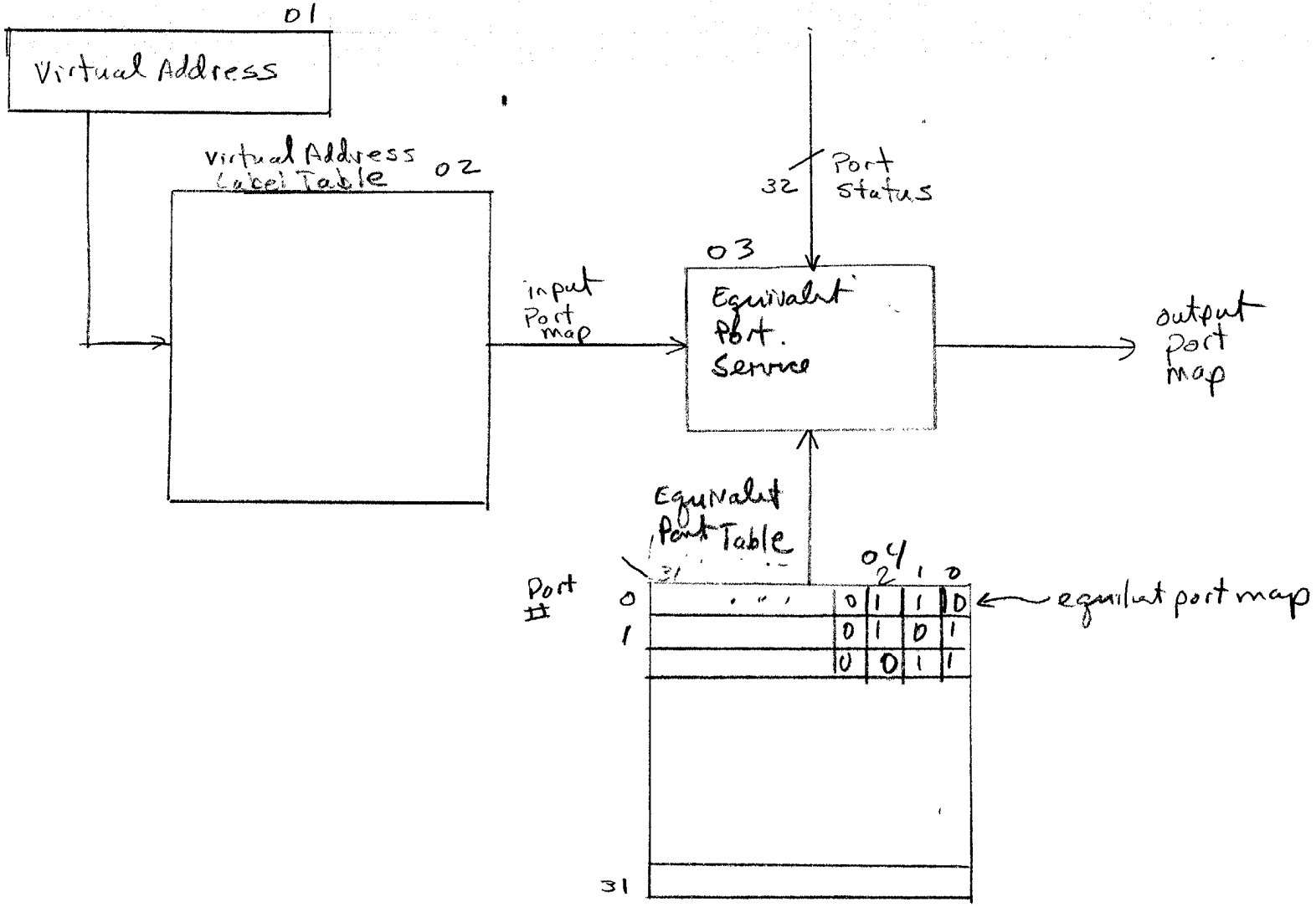


Fig 13

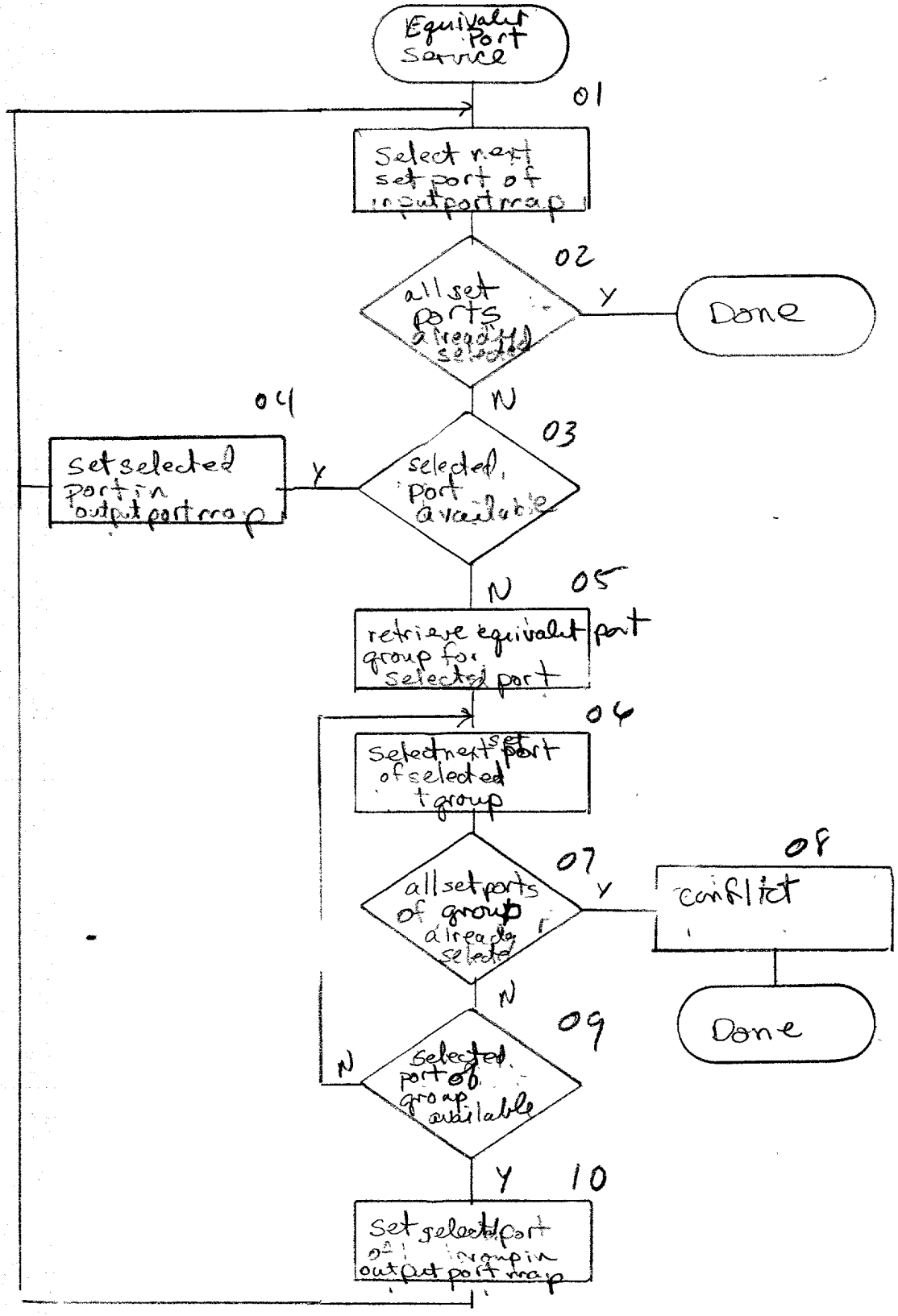

Equivalent Port Service
01
Select next set port of input port map
02
all set ports already selected
Y
Done
N
03
selected port available
N
05
retrieve equivalent port group for selected port
04
Select next set port of selected group
07
all set ports of group already selected
Y
06
conflict
Done
N
09
Selected port of group available
N
Y
10
Set selected port in input port map
04
set selected port in output port map
Y

Fig 14

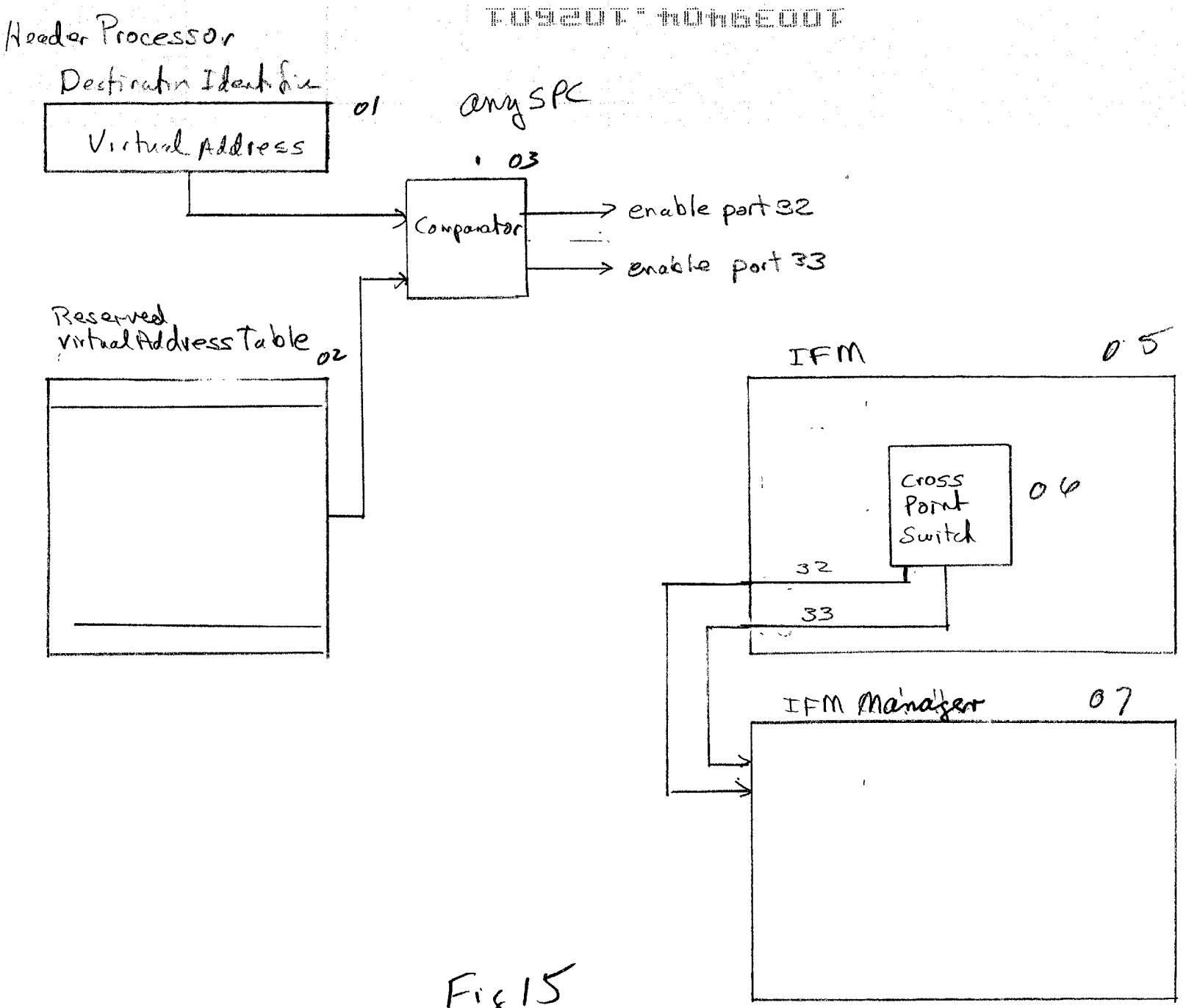
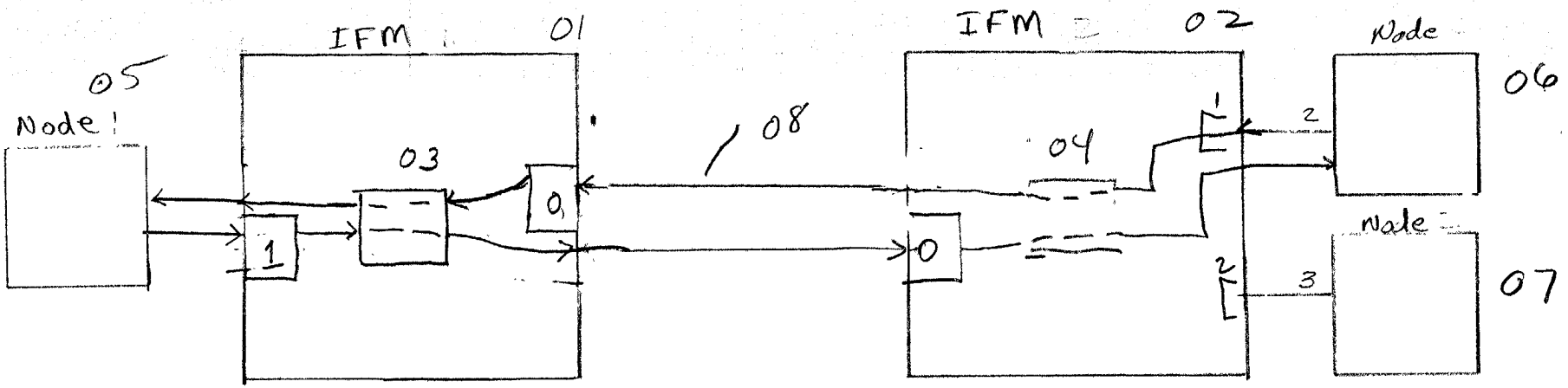

Header Processor
Destination Identifier
Virtual Address
01
any SPC
03
Comparator
enable port 32
enable port 33
Reserved
virtual Address Table
02
IFM
05
Cross
Point
Switch
06
32
33
IFM Manager
07

Fig 15

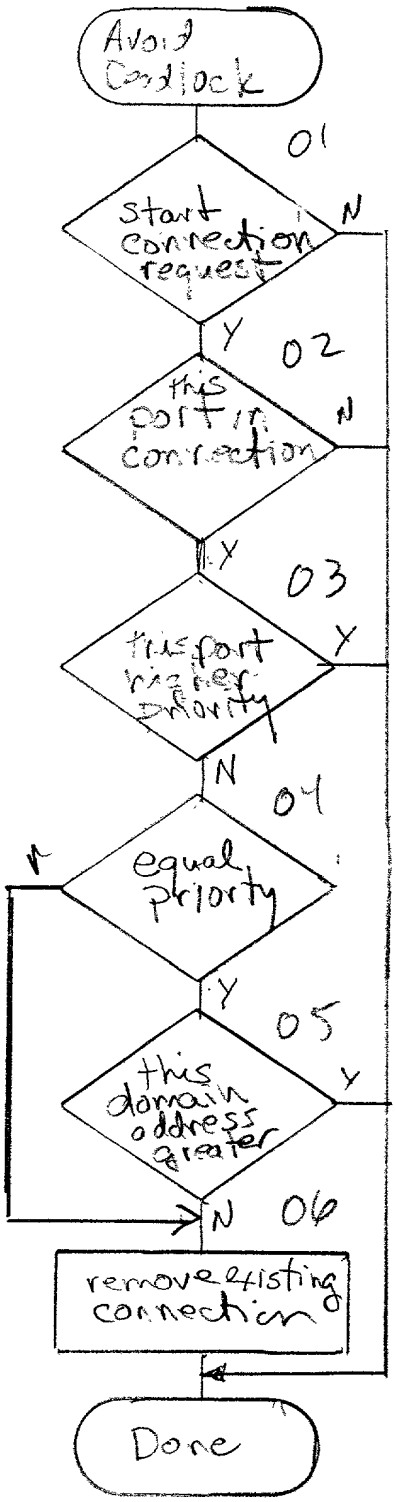


Deadlock

10

Time	Node 1605 IFM 1601	Node 1606 IFM 1602
0	Send start connect 1 3	Send start connect
1	Connect 1 ↔ 0	Connect 2 ↔ 0
2	Forward start connect	Forward start connect
3	Can't forward start connect Node 1	Can't forward start connect

Fig 16



When end-to-end not established

Fig 17

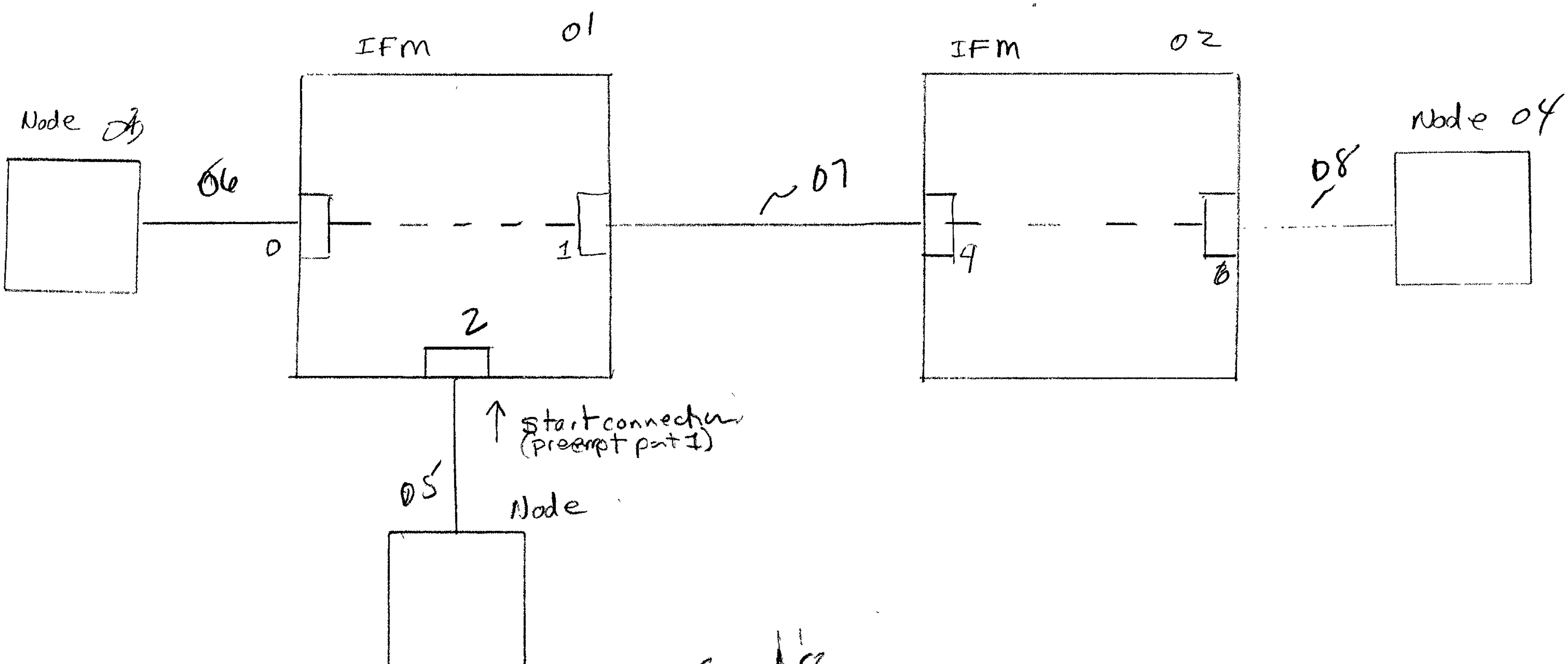

IFM
01
IFM
02
Node
Node 04
06
07
08
05
0
1
2
4
8
Node
start connection
(preempt port 1)

Fig 18

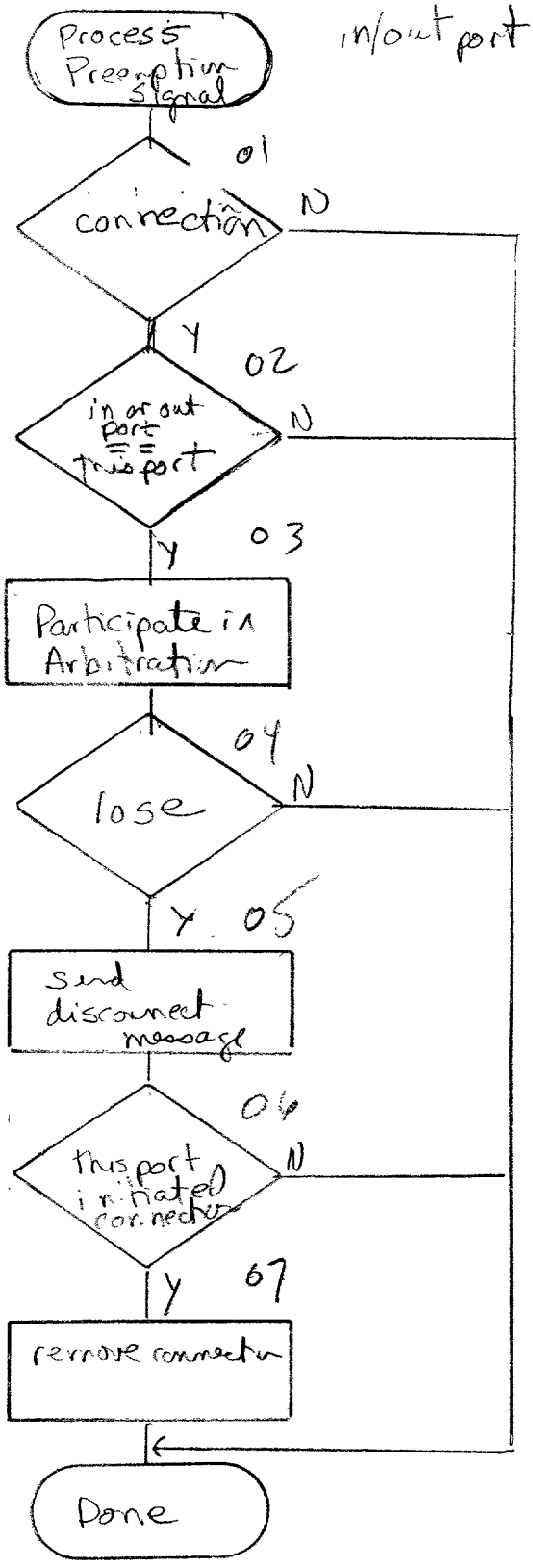

Process Preemption Signal
in/out port
01
connection
N
Y
02
in or out port == this port
N
Y
03
Participate in Arbitration
04
lose
N
Y
05
send disconnect message
06
this port initiated connection
N
Y
07
remove connection
Done

Fig. 19

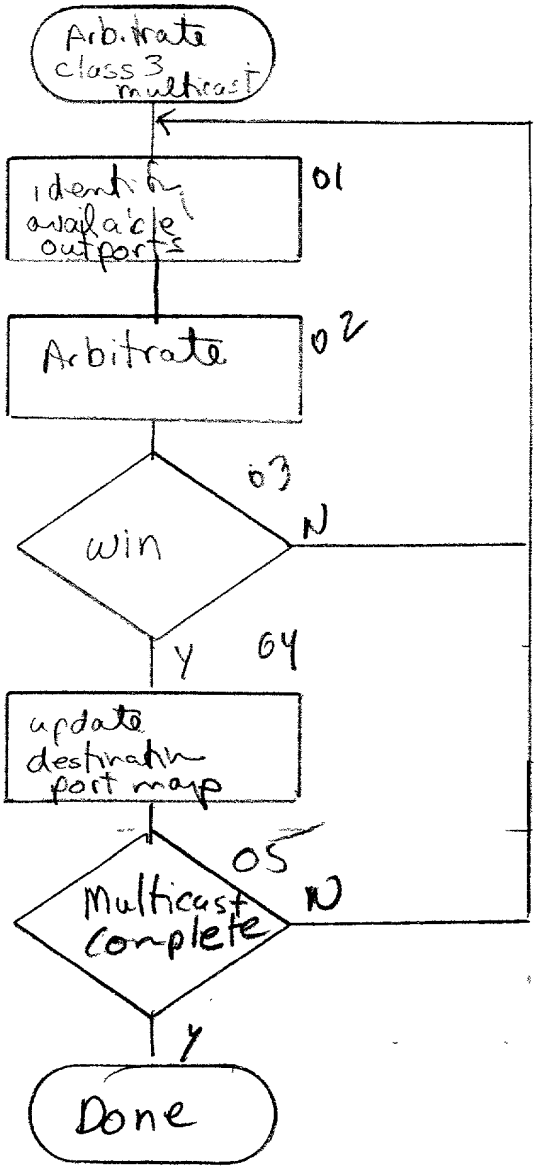

Arb. rate class 3 multicast
identify available outports
01
Arbitrate
02
03
win
N
Y
04
update destination port map
05
Multicast complete
N
Y
Done

Figure 20